REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	28 May 1993	Final Report

4. TITLE AND SUBTITLE

Controller for Fiber Optic Interferometer

5. FUNDING NUMBERS

F6170893W0336

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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8. PERFORMING ORGANIZATION REPORT NUMBER

SPC-93-4016

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

EOARD
PSC 802 BOX 14
FPO 09499-0200

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

SPC-93-4016

11. SUPPLEMENTARY NOTES

Attached is the progress report "Report on Design, Construction, and Testing of Prototype" which is needed for a complete report.

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This report lists the items which comprise the delivered phase controller, and gives instructions for its testing and use. It assumes familiarity with the progress report "Report on Design, Connstruction, and Testing of Prototype."

14. SUBJECT TERMS

15. NUMBER OF PAGES

30

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19, SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Special Contract SPC-93-4016

Controller for Fiber Optic Interferometer

Final Report

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28th May 1993

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1 Scope of report

This report lists the items which comprise the delivered phase controller, and gives instructions for its testing and use. It assumes familiarity with the progress report 'Report on design, construction, and testing of prototype', hereafter referred to as *Progress Report*.

2 List of hardware

The prototype MFPC was converted into the deliverable model by following the steps outlined in *Progress Report*, §5. The following items are supplied as the final deliverable:

1. The final report (this document);
2. The main box, containing modules: LV PSU, HV PSU, HV AMP, SUM/DIFF, AMPLIFIER (2 off) and REFERENCE;
3. The servo box, containing modules: SWEEP, SKIP, RESET, MOD, SERVO, INT1 ($\int$), INT2 ($\int\int$), PROP and DERIV;
4. 1 off 7-pin DIN cable, to supply servo box with power from main box;
5. 2 off 3-pin DIN cable, for power supply to detectors.
6. 2 off detector units, each comprising: 'very sensitive current amplifier', detector head, and mini-BNC cable;
7. 1 off US-style mains lead.

3 Notes for use

This section must be read before the unit is switched on.

The following points must be observed for correct and safe operation of the MFPC:

1. The mains supply to the unit must be 115 V AC, 50–60 Hz. It is not suitable for use with the UK mains supply.
2. THE UNIT MUST BE EARTHED VIA THE MAINS SUPPLY CABLE BEFORE SWITCHING ON.
3. The main box must be correctly oriented before switching on—see 'this way up' label on rear panel. This is required for correct operation of relays in HV PSU interlock.
4. The output from the high voltage amplifier HV AMP can be lethal. Do not enable the HV PSU unless the HV AMP is being used. Do not leave conductors connected to HV AMP output exposed.
5. Fuses should only blow due to incorrect use. If a fuse blows, always:
   (a) Ascertain reason for fuse blowing before replacing fuse;
   (b) Replace fuse with one of identical rating;
   (c) Replace front-panel mounted fuses with slow-blow fuses.
6. Signal outputs must not be shorted together or connected to low-impedance sources as this may destroy the output stage. Care must be taken not to confuse inputs and outputs.
7. Input signals should be restricted to the range ± 15 V. Higher levels may damage inputs.
8. Keep the lengths of all signal cables as short as possible. Loading with of cables longer than 2 m may affect output signal levels.
9. Many of the circuits use static sensitive devices. If any of the boxes are opened, observe normal handling procedures for such devices.
10. Power must only be applied to the detectors using the 3-pin DIN cables provided, or using cables known to be equivalent. 3-pin DIN cables of *both* wiring conventions are commonly in circulation. The detectors are not protected against application of power with reverse polarity.
11. Check the polarity of PZTs before connecting to the HV AMP. The HV AMP output is always positive. Reverse polarity can de-pole PZTs.

4 Electrical evaluation of controller

Before the MFPC is incorporated into a phase-locked interferometer, the user should become familiar with the function of each constituent module and should check that they each function correctly. The function of each module is described in *Progress Report*, §2. This section describes how to check each module.

The front and rear panel layouts sre shown in figures 7 and 8, for reference.

You will need:

- An oscilloscope: preferably a digital storage 'scope.
- A signal generator with adjustable DC offset.
- A set of BNC cables.

4.1 Main box

The function of each module in the main box is self-evident and testing is straightforward.

4.1.1 Mains Supply

Initial settings: the main box and servo box should *not* be connected together at this stage. MAINS switch should be off (out). LV PSU and HV PSU switch should be switched OFF.

Plug the main box into the mains supply (115 V AC, 50–60 Hz) using the mains cable provided. THE MAINS SUPPLY MUST BE EARTHED. Press the 'mains' button. The neon indicator should light up.

4.1.2 Low voltage supply—LV PSU

Switch on. Both LEDs should light.

4.1.3 Reference—REFERENCE

Monitor output on CRO and adjust trimmer 'adj'. Check that each switch setting provides a DC output in the range specified in the *Progress Report*.

4.1.4 Amplifiers 1 & 2—AMPLIFIER

Check operation as amplifier for signals up to 100 kHz. Small signal bandwidth is >1 MHz but may be slew-limited for large signals at the higher frequencies.

4.1.5 Sum and difference amplifier—SUM/DIFF

Put the same signal into both inputs and check output for both switch settings. Small signal bandwidth is >1 MHz but may be slew-limited for large signals at the higher frequencies.

4.1.6 High voltage supply—HV PSU

Setting the HV PSU supply voltage: The output voltage of the HV PSU is set by HV TRIM. This should be adjusted while monitoring the ÷50 output of the HV AMP on the CRO. Use the signal generator or the REFERENCE output to supply the HV AMP input with around 11 V DC. Adjust HV TRIM to give the desired maximum voltage at the HV AMP output. Settings beyond 300 V (6 V on ÷50) are not recommended.

4.1.7 High voltage amplifier—HV AMP

Having set the HV PSU supply voltage as above, set the signal generator to give a signal consisting of a low frequency ($\ll$1 kHz) signal superimposed on a positive DC offset, so that the sgnal is always positive. Connect this to the HV AMP input and monitor the ÷50 output on the CRO. Apparent gain should then be 0.6. The CLIPPING LEDs should light when the output nears the supply rail level.

Gain should not be affected by loading the output with a PZT transducer or a low value capacitor. Output current limiting may be observed by loading the output with a 2.2 μF capacitor and driving at 200 Hz.

The HV AMP has a 51 Ω resistor in series with the output. It may be necessary to add a larger resistor, of a few hundred ohms, in series with some PZTs to reduce high frequency noise and increase servo stability. Use only non-inductive (i.e. not wirewound) resistors for this.

4.2 Servo box

Initial settings: MOD: DISABLE; SERVO: OFF; INT1, INT2, PROP & DERIV: OFF. Connect the servo box to the main box using the 7-pin DIN cable supplied.

Monitor SERVO O/P on oscilloscope. If the HV AMP is to be used, then with SERVO I/P disconnected, adjust OUTPUT OFFSET to give around 5 V at O/P. Otherwise, adjust this to give whatever bias is required at the input of the phase modulator used.

4.2.1 SWEEP & SKIP

Depressing SWEEP and SKIP should give traces similar to those shown in figures 6 and 7 of *Progress Report*. Adjust OFFSET, RATE, and DURATION presets and check that the output is modified accordingly. Ranges of adjustment are given in *Progress Report*.

4.2.2 Modulation—MOD

Connect a signal generator to MOD I/P. Enable MOD. The SERVO O/P should show this signal added to the offset set in §4.2, with no significant leakage below 10 kHz when MOD is disabled. Check that LEVEL varies attenuation.

4.2.3 INT1 ($\int$) & INT2 ($\int\int$); setting offsets; HOLD and RESET

Connect a DC level to SERVO I/P. Enable SERVO and INT1. Hit RESET and observe linear ramp at output, as shown in first part of figure 1, *Progress Report*. Vary DC level and INT1 gain to vary rate of ramp. Switch SERVO to INV and observe ramp in opposite direction.

Disable INT1 and enable INT2. Hit RESET and observe quadratic ramp at output, as shown in first part of figure 2, *Progress Report*.

Apply HOLD and RESET during sweep to obtain traces as in figures 1, 2, and 5 of *Progress Report*.

Setting offsets Ideal integrators would give zero drift with SERVO I/P grounded. INT1 and INT2 both have offset trimmers, which will be correctly set before shipping to minimise drift. These can be adjusted as follows:

1. INT1:
   (a) Short out SERVO I/P with $50\,\Omega$ termination.
   (b) Enable SERVO and INT1. Set gain to mid-range on $\times 0.1$.
   (c) Hit RESET and observe slow drift at SERVO O/P.
   (d) Adjust trimmer OS1 to null drift.
   (e) Increase gain to $\times 1$ and repeat.
   (f) Increase gain to $\times 10$ and repeat.
2. INT2: as for INT1, but disable INT1 and enable INT2. OS2 adjusts initial slope of drift, OS1 adjusts curvature.

4.2.4 PROP and DERIV

Apply a 100 Hz sinusoidal signal to SERVO I/P. Disable INT1 and INT2 and enable PROP. PROP should behave as a simple amplifier, with HOLD acting as sample-and-hold.

Apply a 5 kHz sinusoidal signal to SERVO I/P. Disable PROP and enable DERIV. The output should have a $\pi/2$ phase lead with gain proportional to frequency. HOLD should act as sample-and-hold.

4.2.5 Trigger signals

The trigger inputs of SWEEP, SKIP, RESET, and HOLD may be used both as inputs and outputs, with certain restrictions:

Use as input: external triggering, for remote or automated operation, is by negative-going TTL edge or pulling the input to ground. These inputs can thus be driven by open-collector logic or opto-isolators, provided that the driver used can sink 1 mA. Triggering can also be done by an external switch shorting the input (the inputs are internally debounced), or driven by the TTL output of a signal generator or pulse generator. Use of opto-isolators is recommended for trigger signals obtained from computers, to avoid pickup of EMI.

Use as output: TRIGs give negative-going TTL edge on trigger, pulled back up to +5 V by a $10\,\mathrm{k}\Omega$ resistor when trigger released. Suitable for driving inputs of impedance $> 100\,\mathrm{k}\Omega$. This is intended for triggering oscilloscopes.

4.3 Detectors—Mounting and grounding

The shielded enclosures of the detector heads are grounded to the shield of the connecting co-axial cable. To minimise electrical pick-up, the detector head should otherwise be electrically isolated. The head is supplied with no mounting point—its lid should be removed and drilled to accept an insulated mount. In the absence of any in-house standard, a 12 mm insulating post, centrally drilled and tapped M6 is an ideal mounting post. The lid should then be drilled with a central 6.5 mm dia. hole.

Lowest pickup is achieved when the detectors are powered by their internal batteries, and operated over a grounded optical bench.

If problems with pickup persist, then the connection between cable-shield and case-ground in the detector head can be severed and the head enclosure grounded separately. Similarly, the case of the transimpedance amplifier can be floated by removing the internal red jumper, allowing it to be grounded separately.

5 Use as phase controller

This sections refers to notation and definitions given in appendix A, which should be read before proceeding. Appendix A contains a general discussion of the basics of phase control in fibre optic interferometers. Oscilloscope traces of typical signals obtained from a phaselocked interferometer are given in *Progress Report*.

5.1 General description

A general schematic of how to configure the MFPC as a phase controller is shown in figure 1. Here, the servo box performs the function of loop filter $G(s)$.

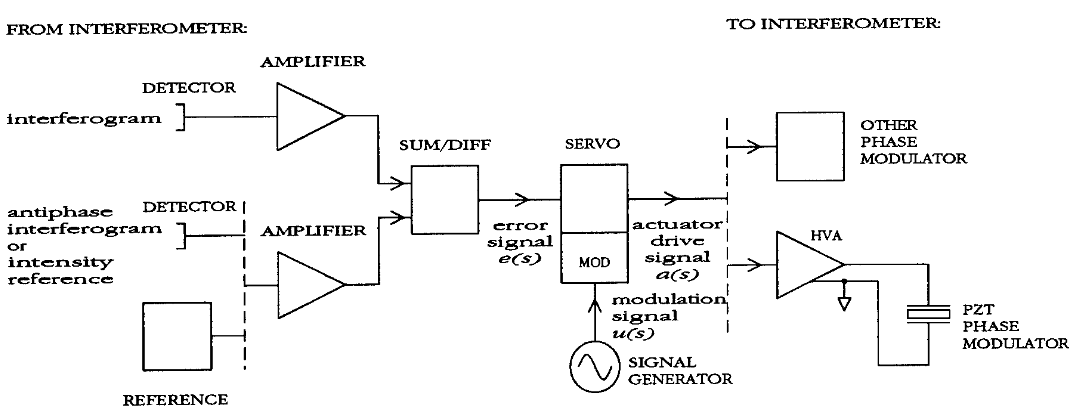

Figure 1: General schematic of MFPC (phase modulators not supplied)

The error signal may be generated by subtracting the interferogram signal from an intensity reference, from an antiphase interferogram, or from an internally-generated voltage reference. The servo output may be used to drive a PZT phase modulator via the HV AMP, or may drive any other phase modulator which accepts input signals in the range ±15 V.

The simplest configuration for the phase controller is shown in figure 2, for HVA and PZT phase modulator, or figure 3 using a different phase modulator and driver. A DC offset (reference signal) is added to the signal from the detector (correction signal) to give an error signal, which the servo attempts to maintain at zero. This gives good phase control when the reference intensity is well away from the extrema of the interferogram. The error signal is passed through the loop filter, i.e. the SERVO box, to give an actuator drive signal. This drives the actuator (the PZT), which changes the phase difference in the interferometer, changing the output intensity and hence the detector signal, closing the control loop.

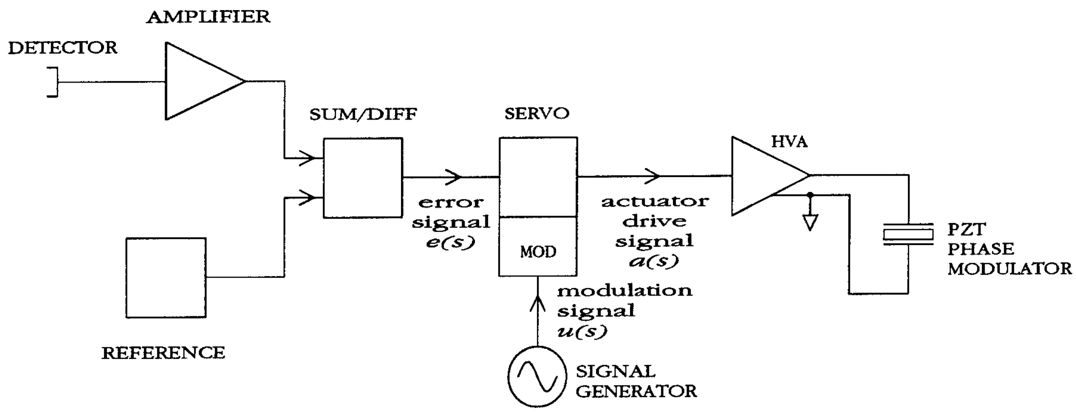

Figure 2: Schematic of MFPC with voltage reference and HVA/PZT

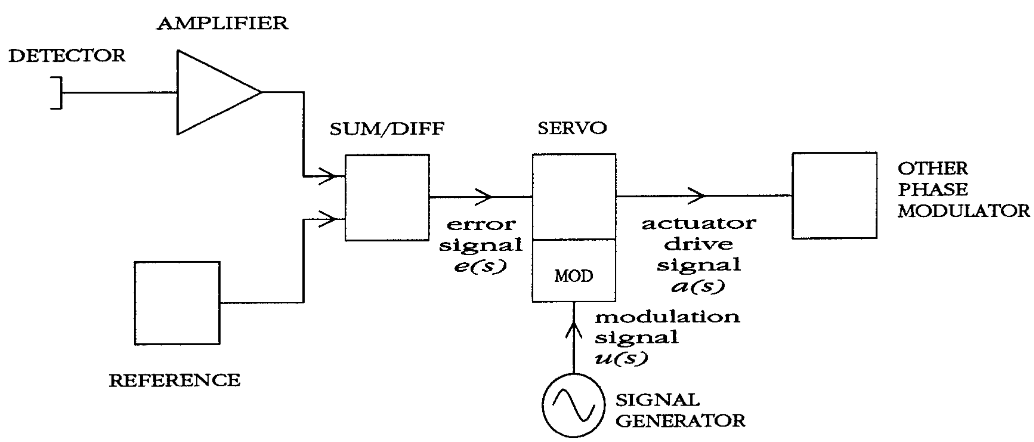

Figure 3: Schematic of MFPC with voltage reference and other phase modulator

5.2 Setting up loop filter

The loop filter parameters for the control system, i.e. the various gain settings, can in principle be set up by measuring the transfer characteristics of the various stages and calculating and setting the ideal parameters for the chosen loop filter, given some criteria on stability and bandwidth. In practice however, it is usually easiest to take the following 'hands-on' approach:

1. Use a single integrator with minimum gain as loop filter (type 1.)
2. Hit RESET. The interferometer should lock-up, i.e. the phase should stabilise at a constant value.
3. Increase gain of integrator until the system becomes unstable.
4. Reduce gain to regain stability, hit RESET.

This process is described in more detail in §5.3.

If better low-frequency rejection (or zero velocity error) is required, then type 2 control can be obtained by enabling INT2 set to its minimum gain, in addition to INT1, and a similar procedure followed to increase and set the gain of INT2. PROP and DERIV are often useful in improving the high-frequency response and extending the servo bandwidth, to compensate some of the limitations of the actuator, but should initially be left disabled.

5.3 Detailed instructions for a specific case

In order to phaselock the system at quadrature with a voltage reference:

1. Set the system up on an interferometer, using a narrowband source, connecting the MFPC as shown in figure 2 or figure 3.
2. Monitor error signal and control signal on oscilloscope.
3. Disable SERVO and all loop filters (INT1...DERIV). Set the integrator gain to minimum (both knobs clockwise). Set the signal generator to produce a triangular wave at $\sim 1\,\text{Hz}$, and enable MOD.
4. The detector signal should show a set of interference fringes, similar to those in figure 4. Adjust the detector and amplifier to give fringes of around 2 V. The error signal should look similar, but be shifted by a DC level. Adjust the level of the reference signal to centre the error signal fringes about 0 V, as shown in figure 4.

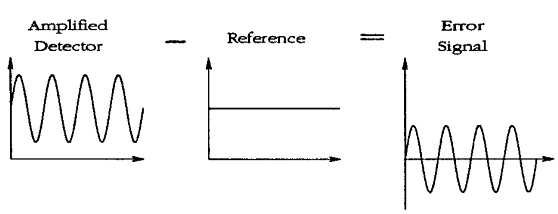

Figure 4: Detector, reference and error signals

5. Disable the MOD. Enable SERVO and INT1. Hit RESET. The interferometer should now lock up. Hit RESET whenever the the actuator drive signal (SERVO O/P) latches up to the supply rails.

6. Increase the gain of INT1 until the system becomes unstable, shown by the error signal going into oscillation. Back off the gain until stability is regained, and hit reset. Once a stable setting has been obtained, the gain controls should no longer need adjusted. Increases in detector signal level will, however, change the point of phase-lock.

5.4 Other cases

Using an intensity reference instead of a voltage reference stabilises the reference phase against drifts in the power of the light source. This is achieved by connecting up as shown in figure 5.

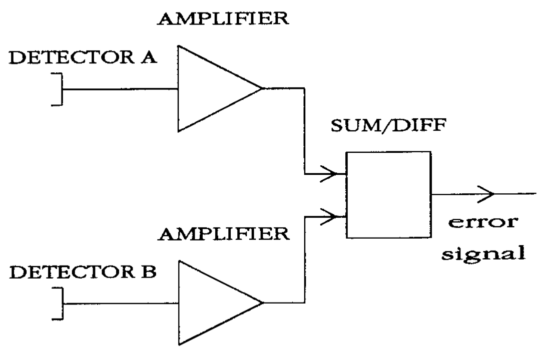

Figure 5: Connections for antiphase inputs

Similarly, if the two antiphase outputs of the interferometer are detected, then the same arrangement gives zero error signal at phase quadrature, and can be used to phase-lock the interferometer about this point.

Once the interferometer has been locked up about some phase, SWEEP and SKIP can be used to scan through and step through the interferogram. After a SWEEP, the control system should lock up again at the same phase as before the scan (*Progress Report*, figure 10.) After a SKIP, the control system should lock up an integral number of fringes away from the original point (*Progress Report*, figure 11.)

With the correct settings of RATE and DURATION, repeatedly hitting SKIP and switching POLARITY should allow the point of phaselock to be stepped up and down the interferogram.

5.5 Broad band interferometry

The MFPC can be used to generate interferograms with broad band sources by either:

- Phaselocking to a separate narrowband metrology beam in the interferometer, with separate detection of the signal and metrology interferograms;

- Phaselocking near to the centre of the broadband interferogram and using SWEEP to make a broad scan over the interferogram.

5.6 Other means of phase measurement

Homodyne interferometers often use more complicated phase measurement techniques, such as dithering with measurement at harmonics, and phase stepping. Such schemes are easily incorporated into the MFPC by inserting suitable signal processing between the detectors and the SERVO I/P.

A Phase control in fibre optic interferometers

A.1 General principles

A schematic of the control system for a two-beam fibre optic interferometer is shown in figure 6. The control system response will be considered in the s-domain [1], i.e. in terms of the Laplace Transforms of signals and transfer functions.

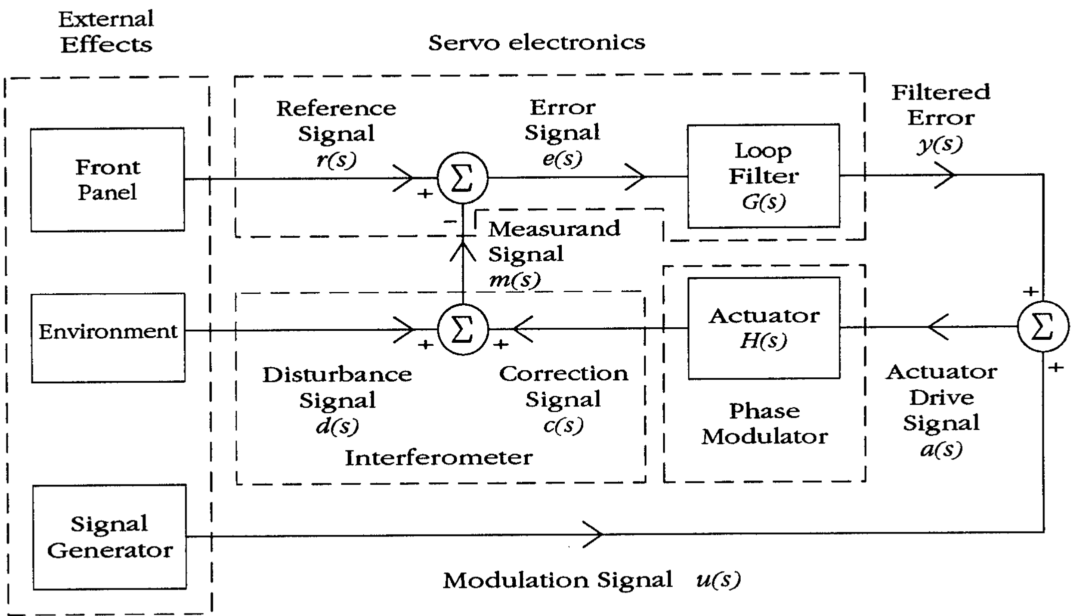

Figure 6: Schematic of servo system

The *disturbance signal* $d(s)$ represents the phase difference between the recombining beams when the phase modulator is in some initial static state. $d(s)$ thus includes the intrinsic static phase bias in the interferometer and phase shifts due to environmental effects such as changes in temperature, pressure, and strain. The *correction signal* $c(s)$ is the phase shift produced by the phase modulator. The disturbance and correction signals combine to give the *measurand signal* $m(s)$ which is the total phase difference between the recombining beams:

$$m(s) = d(s) + c(s) \tag{1}$$

The measured phase signal is subtracted from the *reference signal* $r(s)$ in the servo electronics to give an *error signal* $e(s)$:

$$e(s) = r(s) + m(s) \tag{2}$$

The servo tracks the measurand signal with the reference signal by applying feedback to null the error signal. Feedback is applied via the loop filter and actuator, which have transfer functions $G(s)$ and $H(s)$ respectively. A *modulation signal* $u(s)$ may be added to the *filtered error* $y(s)$ to give the *actuator drive signal* $a(s)$. The modulation signal is useful for setting up and testing the servo system.

In a simple homodyne interferometer, the measured signal is usually an intensity and so is only a good linear approximation to phase ϕ when phase is in the range $(n+\frac{1}{4})\pi < \phi < (n+\frac{3}{4})\pi$, i.e. within $\pi/4$ of a quadrature point.

The purpose of the control system, that is the feedback applied by the combination of loop filter $G(s)$ and actuator $H(s)$, is to null the error signal over the range of frequencies where the disturbance signal is significant. The relationship between the error signal and the other signals is easily found:

$$
\begin{aligned}
e(s) &= r(s) - m(s) & (3)\\
&= r(s) - d(s) - m(s) & (4)\\
&= r(s) - d(s) - H(s)m(s) & (5)\\
&= r(s) - d(s) - H(s)(u(s) + y(s)) & (6)\\
&= r(s) - d(s) - H(s)u(s) - H(s)G(s)e(s) & (7)
\end{aligned}
$$

$$\Rightarrow \quad e(s) = \frac{r(s) - d(s) - H(s)u(s)}{1 + H(s)G(s)} \tag{8}$$

Accurate phase tracking requires high rejection of disturbances. Putting $D(s) = 1 + H(s)G(s)$ and $M(s) = 1/D(s)$, then $|D(s)|$ should be large and hence $|M(s)|$ small over the required bandwidth. Noise will be amplified at any frequency for which $|D(j\omega)| < 1$, and the system will be unstable (marginally stable) if $|D(j\omega)| = 0$ ($|D(j\omega)| \simeq 0$) for any frequency ω. $H(s)G(s)$ is known as the *closed loop transfer function.* For any frequency ω, where $s = j\omega$, $H(s)G(s)$ must never take the value -1, and ideally should stay outside the unit circle centred on -1. Consult [1] or any other standard control text for further discussion of equation 8 and for basic control theory.

A.2 Ideal actuator and servo type

The *type* of the loop filter defined as the lowest power of s in the denominator. In the low-frequency limit, the error signal for a type n loop filter is proportional to the nth derivative of the disturbance signal. Hence:

type 0 control (proportional control only) gives a non-zero error even for steady-state disturbances;

type-1 control gives a zero steady state error for static disturbances but a non-zero error for constant-velocity (ramp) type disturbances;

type-2 control gives a zero steady state error for static and constant-velocity disturbances but a non-zero error for constant-acceleration type disturbances.

With an ideal actuator, $H(s)$ would be a constant, independent of s, converting voltage into optical phase. Then, if a single integrator (INT1) is used in the feedback loop, a type-1 open loop transfer function is obtained

$$G(s)H(s) = \frac{K}{s} \tag{9}$$

If both single (INT1) and double (INT2) integrators are used in parallel, a type-2 open loop transfer function is obtained

$$G(s)H(s) = \frac{K_1}{s} + \frac{K_2}{s^2} \tag{10}$$

$$= \frac{sK_1 + K_2}{s^2} \tag{11}$$

A.3 Limitations of real actuators

In the type-1 and type-2 control systems described above, gain, and hence bandwidth, could be increased without limit. Real actuators have a finite bandwidth, and the resultant shifts in phase and amplitude restrict the range of gain over which the control system is stable.

If the actuator has a simple m-th order rolloff above some frequency ω_a, then it it usually sufficient to have the open loop gain drop below unity at some lower frequency ω_b. However, piezoelectric actuators are often strongly resonant, giving a strong peak in $H(j\omega)$ accompanied by strong phase shifts. It is then often necessary to roll off the open loop gain at a much lower frequency, so that its value does not near unity around resonance.

References

[1] R. C. Dorf *Modern Control Systems* Sixth Edition, Addison Wesley, New York, 1992.

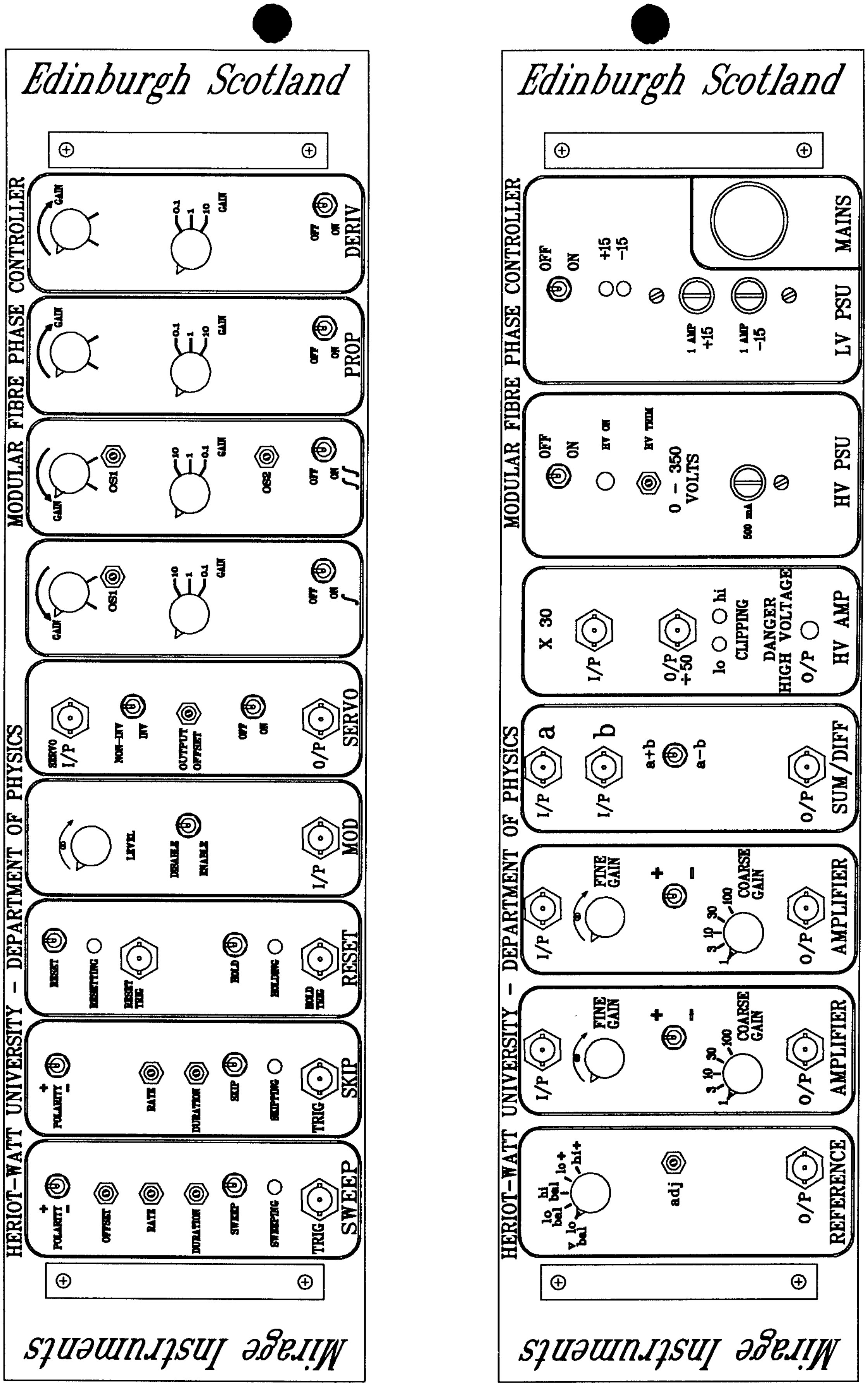

Figure 7: Front panel layout

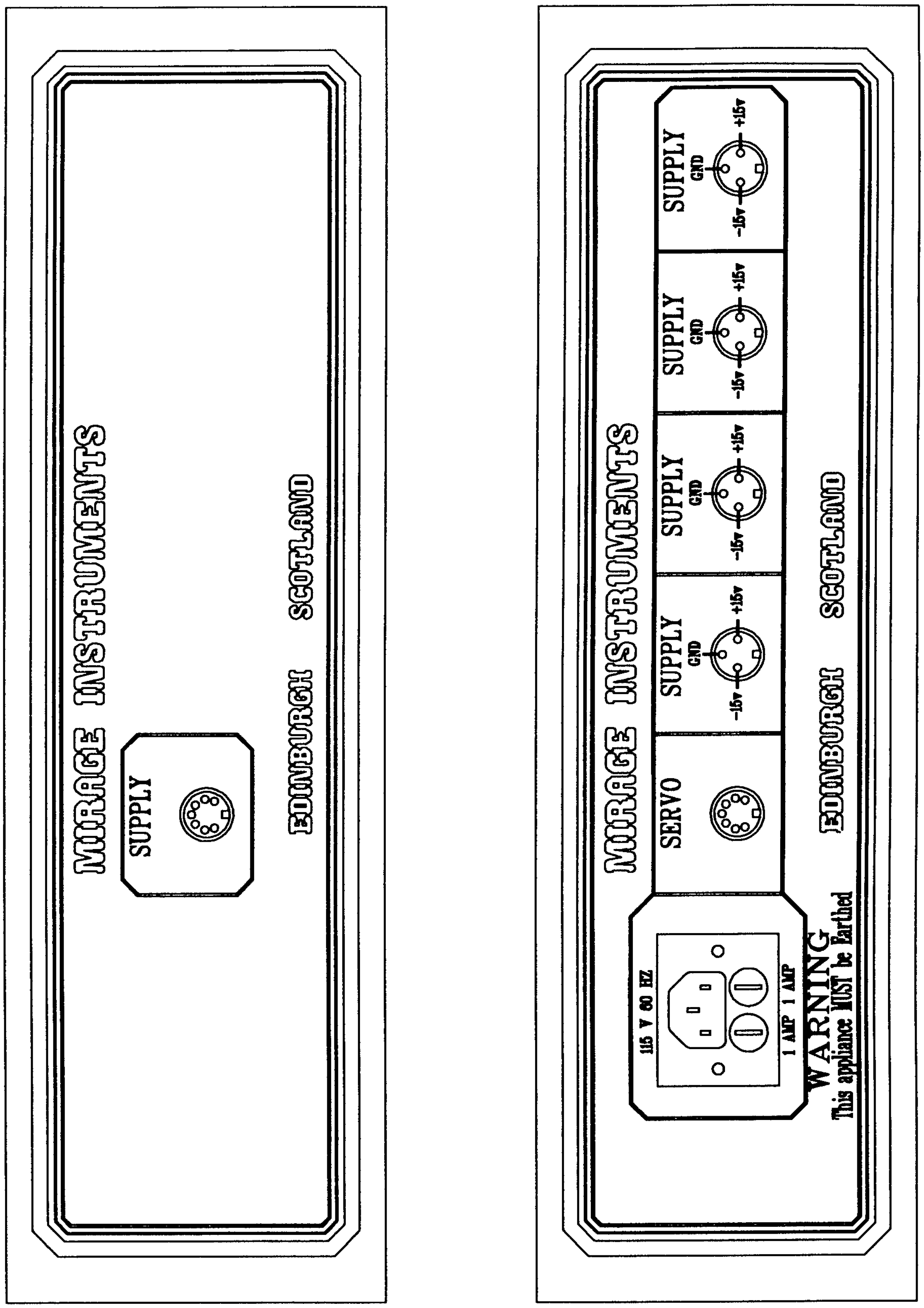

Figure 8: Rear panel layout

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Controller for Fiber Optic Interferometer

Report on design, construction, and testing of prototype

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7th April 1993

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List of Figures

1 Scope of report

This report covers the design, construction and testing of a phase controller for optical fiber interferometers. Instructions for its use will form part of the final report, which will accompany the delivery of the final version of the phase controller.

2 Description of controller

A prototype Modular Fibre Phase Controller (MFPC) has been designed. The MFPC consists of a main box, a servo box, and two detectors.

2.1 General description

The main box comprises input and output signal conditioning modules and power supplies and is powered from the mains supply. It was based as far as possible on existing circuit designs.

The servo box incorporates all of the functions directly related to the control system. It is virtually a completely new design, as previous servo units used in house were not sufficiently flexible in design to incorporate the required new features. Power is supplied to the servo unit via a 7 core cable running from the main box. This cable also connects the chassis of the two boxes.

The detectors operate independently of the main and servo boxes. They may be powered by internal rechargable Nickel-Cadmium (Ni-Cad) batteries or by the ± 15 V supply available from the main box. The Ni-Cads trickle charge from this supply when connected.

A modular approach to construction has been taken, distinct functions being performed by separate boards. Individual boards may be thus be disconnected without affecting the operation of other boards and modification or replacement of boards is straightforward. The front panels are produced as single items, and so are not readily modified.

2.2 Main box

2.2.1 Mains Supply

Mains electricity must be supplied via the rear panel IEC connector. This connector is fused. A US-style mains cable is supplied. A mains filter and front-panel front panel pushbutton mains switch are included. The mains supply must be 115 V, 50–60 Hz. THE MAINS SUPPLY MUST BE EARTHED. The chassis of the main box is earthed via the mains supply.

2.2.2 Low voltage supply—LVPSU

Purpose: to provide:

- ± 15 V for internal and external use, protected by two front-panel mounted 1 A fuses. Four ± 15 V outputs are provided by 3-pin DIN connectors on the rear panel.

- +5 V DC for internal use only.

A single front panel switch both supplies.

2.2.3 High voltage supply—HVPSU

Purpose: high voltage supply for HVA.

Providing 0 V to +300 V DC, set by front panel preset, with a foldback current limit of 60 mA short circuit, 220 mA at 300 V. Interlocked to low voltage supply and enabled by front panel switch. Controls allow voltage up to 350 V, but may suffer from ripple when supplying high current at above 300 V. Presence of high voltage is indicated by neon panel indicator.

2.2.4 Reference—VREF

Purpose: reference level for single output interferometer.

Generates a reference voltage with level adjusted by front panel trimmer. Front panel switch sets voltage ranges (approximate):

Setting	Range		
v lo bal	-44 mV	–	+44 mV
lo bal	-1 V	–	+1 V
hi bal	-11 V	–	+11 V
lo +	0 V	–	+1.6 V
hi +	0 V	–	+11 V

2.2.5 Amplifiers 1 & 2—AMPLIFIER

Purpose: to set gain of detector signal before servo input.

Coarse gain 1–3–10–30–100 set by front panel rotary switch. Fine gain 0–1 by front panel multiturn pot, for high resolution. Polarity set by front panel switch (+/-). Bandwidth > 1 MHz. Differential input grounded via PCB jumper. Jumper may be removed to isolate grounds when when ground loops cause problems.

2.2.6 Sum and difference amplifier—SUM/DIFF

Purpose: subtraction of reference level from interferogram or subtraction of antiphase interferograms; to yield centre-zero signal for servo input.

Differential inputs A and B have ground jumper as for AMPLIFIER. Output A+B or A-B; polarity set by front panel switch.

2.2.7 High voltage amplifier—HVA

Purpose: to drive PZT phase modulator.

Gain of +30. Original design bandwidth of 1 kHz was extended to around 4 kHz by a minor modification of the circuit. Minimum output level $\simeq$3 V. Maximum output level set by HVPSU. Current limited to: source 37 mA, sink 30 mA. Current limits set to ensure adequate heat dissipation at maximum load. The HV output is via an SMB connector, to avoid risk of swapping high and low voltage cables. A separate buffered output gives HV output ÷50. 'Clipping' LEDs light when output nears supply rails, signifying signal distortion or saturation of servo. 'Clipping' levels are set by internal trimmers. Output stage bias current also set by internal trimmer.

2.3 Servo box

The servo box is based around the servo master, which accepts the error signal as input and provides the correction signal as output. INT1, INT2, PROP, and DERIV determine the characteristics of the loop filter. RESET temporarily modifies the loop filter state. SWEEP and SKIP both modify the loop filter and the output. MOD modifies the output directly.

2.3.1 Servo master—SERVO

Purpose: input of error signal and output of correction signal.

Differential input has ground isolation jumper as for AMPLIFIER. Polarity of servo set by front panel switch. Output offset of 0 V–5.6 V set by front panel trimmer. Front panel switch enables/disables loop filter. This switch does *not* disable SWEEP, SKIP, or MOD.

2.3.2 Loop filter sections (LFS)—INT1, INT2, PROP, and DERIV

Purpose: to determine servo frequency response and stability.

INT1 ($\int$), INT2 ($\int\int$), PROP, and DERIV respectively, give integral, double integral, proportional and derivative control. Coarse and fine gains are set by front panel rotary switch and log pot. 'Hold' signal generated by 'hold', on RESET and by SWEEP and SKIP, freezes outputs of loop filter sections.

Each LFS may be disabled by a front panel switch. INT1 and INT2 have front panel offset trimmers to null integrator drift. See 'Instructions for use' in final report for instructions on their adjustment.

2.3.3 Modulation—MOD

Purpose: to provide direct modulation of servo output, for testing of servo and interferometer.

Enabled/disabled by front panel switch. Level set by multiturn pot.

2.3.4 Reset and hold—RESET

Purpose: 'reset' zeros loop filter, setting servo to centre of operating range; 'hold' temporarily locks loop filter state, freezing output.

Front panel LEDs indicate operation of 'reset' and 'hold'. Both may be triggered either from front panel switch or external trigger input. The trigger input may also be used as an unbuffered trigger output for data acquisition for both switch and external trigger. External trigger should be active low using open collector TTL or equivalent. See 'Instructions for use' in final report.

'Hold' persists for approximately 10 ms after release of trigger.

2.3.5 Sweep—SWEEP

Purpose: scans servo output with loop filter disabled, to observe local fringe pattern without losing position of servo lock within the interferogram.

SWEEP puts loop filter on 'hold' and modulates the servo output with an offset ramp. At the end of the ramp, the modulation is removed and 'hold' released.

Front panel trimmers control rate, duration and offset of sweep over the approximate ranges:

rate:	0–250 $\mathrm{V\,s^{-1}}$
duration:	11 ms–1.1 s
offset:	0–5.6 V

A front panel switch sets scan polarity. Trigger and LED indication are as for RESET.

2.3.6 Skip—SKIP

Purpose: ramps servo output with loop filter disabled, to shift position of servo lock within the interferogram.

SKIP puts loop filter on 'hold' and modulates the servo output with a ramp. At the end of the ramp, 'hold' is released and the modulation decays very slowly, ($\tau \simeq 2.2\,\mathrm{s}$), so that the servo can track the decay. This skips the position of phase lock over an integer number of fringes, determined by the settings of 'rate' and 'duration'

Front panel trimmers control rate and duration of ramp over the approximate ranges:

rate:	0–560 $\mathrm{V\,s^{-1}}$
duration:	1.1–110 ms

A front panel switch sets ramp polarity. Trigger and LED indication as for RESET.

2.4 Detectors

The two detectors are unbiased BPX-65 PIN photodiodes with transimpedance amplifiers. These photodiodes have an active area of 1 mm^2 and 15 pF capacitance at zero bias. The photodiodes and transimpedance amplifiers are housed in separate enclosures, connected by a 150 mm long mini-BNC cable. The transimpedance amplifiers are battery powered, to minimise electrical pick-up. They may be trickle charged via the 3-pin DIN socket using the ± 15 V outputs from the main box.

The transimpedance amplifiers have 6 sensitivity settings which select feedback resistors in the range 1 kΩ–100 MΩ. Each feedback resistor has a parallel capacitor chosen to avoid response peaking for the capacitance of the detector/lead combination. The transimpedance amplifiers also have gain settings of 1–10–100. Use of high 'gain' rather than 'sensitivity' will typically yield higher noise, but will give higher bandwidth when 'sensitivity' is already high.

3 Construction of prototype

A prototype MFPC was constructed. Each individual module described above was constructed on a separate PCB. The boards were assembled and mounted on dummy front panels, to allow refinement of panel layout. The prototype was powered using 110 V at 50 Hz using a step-down transformer driven from the UK mains supply. Each board was tested individually, and its performance compared with the design goals.

This involved:

- Debugging layout—PCB layouts and components lists were checked for correspondence with design, and corrections made.
- Debugging construction—components and tracks not conforming to design were located and corrected.
- Verifying performance—performance was compared to design goals. This required changing some passive components.
- Appraisal of performance. Actual performance was considered and some design changes made to improve performance and simplify operation. In particular, the HVA met its design bandwidth of 1 kHz but was modified to give 4 kHz.
- Considering the front panel layout and re-drafting to clarify the function of controls.

The prototype was tested as described in the following section.

4 Testing

4.1 Main box

The individual boards of the main box operate independently and so testing was straightforward.

- The LVPSU gave correct ± 15 V and 5 V output;
- The HVPSU gave output adjustable from 4 V to 347 V.
- VREF gave outputs covering the ranges stated in 2.2.4 above.
- Both amplifiers had stated gains, bandwidths $\gg$1 MHz and low noise. Polarity switches inverted output.
- SUM/DIFF gave addition and subtraction with a bandwidth $\gg$1 MHz, with low noise.
- The HVA was initially constructed with a design bandwidth of 1 kHz. This was extended to around 4 kHz to maximise the overall bandwidth of the phase controller. Maximum sink and source currents were measured by loading the output with a 2.2 μF capacitor and observing maximum slew rate. Sink and source limits of 27 mA and 37 mA, respectively, were observed. The output stage bias current was reduced to increase the maximum sink current by around 2.5 mA.

Thermal loading was checked by driving the 2.2 μF capacitor at maximum sink and source currents at around 60 Hz continuously. The rises in temperature of the HVA and HVPSU heatsinks were well within safe limits, the box lid became only slightly warm to touch and no change in performance was observed.

4.2 Servo box

4.2.1 Loop filter sections—INT1, INT2, PROP, and DERIV; 'hold'

Figures 1,2 show the effects of INT1 and INT2 on a DC error signal, and the effect of temporarily applying 'hold' to freeze the servo output. Note that the output continues from its previous position when 'hold' is released.

Figures 3,4 show the effects of PROP and DERIV on a sinusoidal error signal, and the effect of temporarily applying 'hold' to freeze the servo output. Note that the output jumps to its new position when 'hold' is released.

4.2.2 RESET: 'Reset'

Figure 5 shows the effect of a 'reset' on an integrated DC signal.

4.2.3 SWEEP

Figure 6 shows the waveform at the servo output for a single 'sweep'.

4.2.4 SKIP

Figure 7 shows the waveform at the servo output for a single 'skip'.

4.3 Detectors

The detectors use an established design and layout, which has proven to give low noise and low electrical pickup, and operate correctly from both internal and external supplies. The performance of both detectors supplied with the final MFPC be verified before delivery.

4.4 Entire system as phase controller

The entire system was tested as a phase controller for a Mach Zehnder interferometer using a Helium Neon laser source. Different, but functionally equivalent, detectors were used in this test.

4.4.1 HVA as piezo driver

The HVA was driven by a triangular wave and the interferometer fringe pattern recorded. The drive waveform and fringe pattern are shown in fig 8.

4.4.2 Servo control

Phaselocking was achieved using INT1 and using INT1 and INT2 in tandem. For the gains used, adding in proportional and derivative signals made the system unstable. Sufficiently high gain on either INT1 or INT2 also made the system unstable (as it should).

4.4.3 Rest and hold

'Reset' was found to return the servo to the central position. 'Hold' suspended phase lock without a sudden jump in phase, and allowed the output to drift freely.

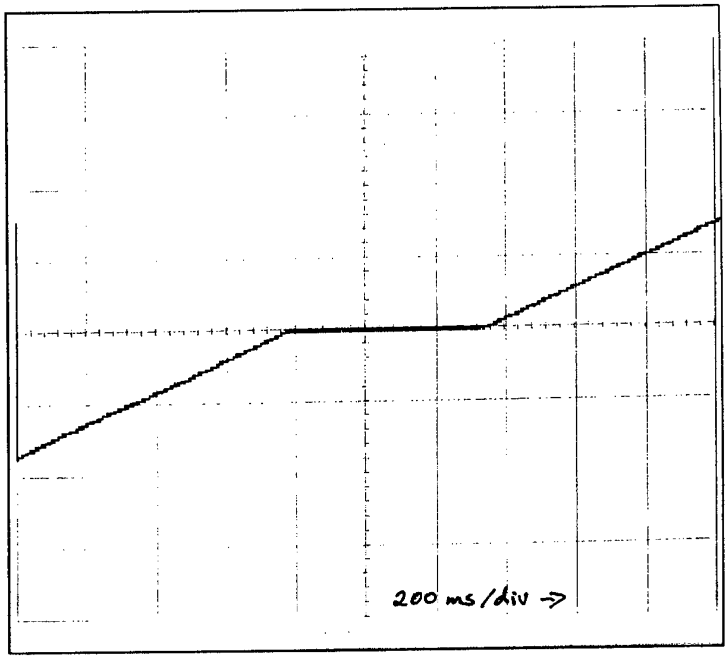

Figure 1: SERVO output: integration (INT1) and 'hold' for a DC error signal

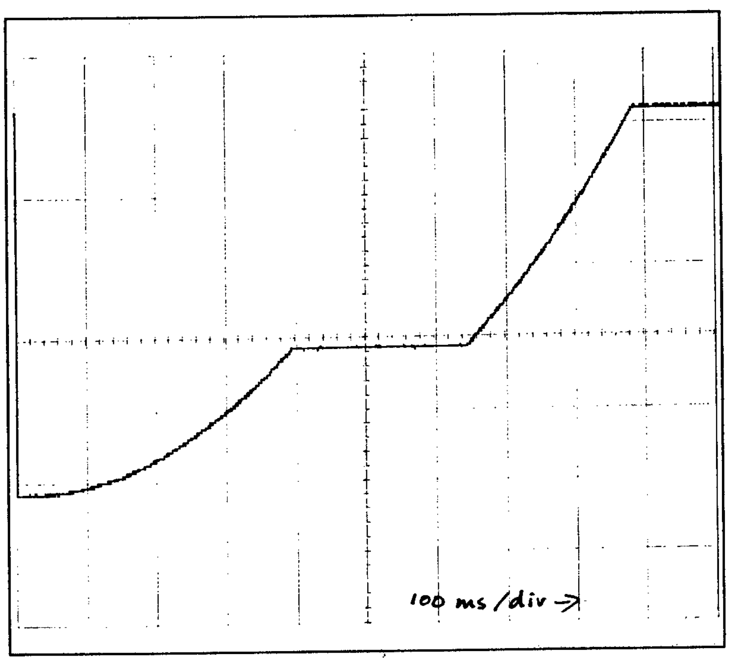

Figure 2: SERVO output: double integration (INT2) and 'hold' for a DC error signal

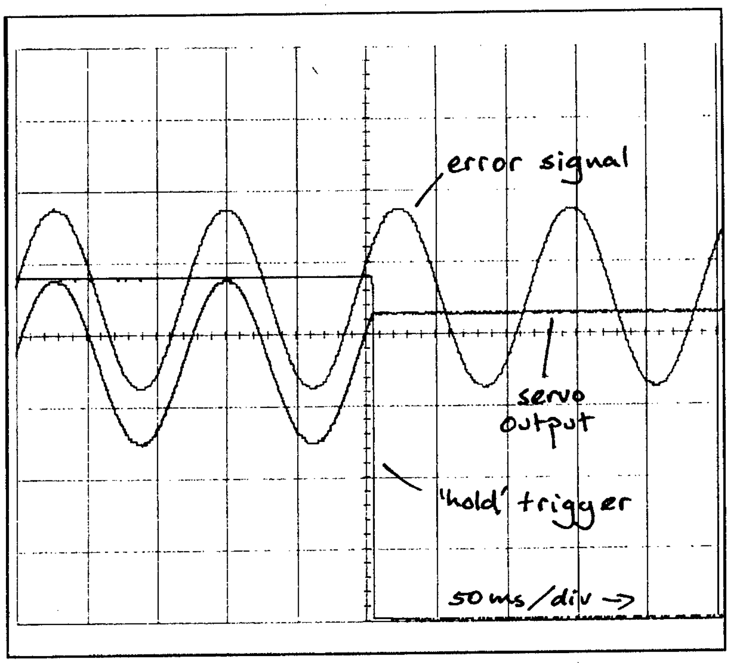

Figure 3: SERVO output: proportional control (PROP) and 'hold' for a sinusoidal error signal

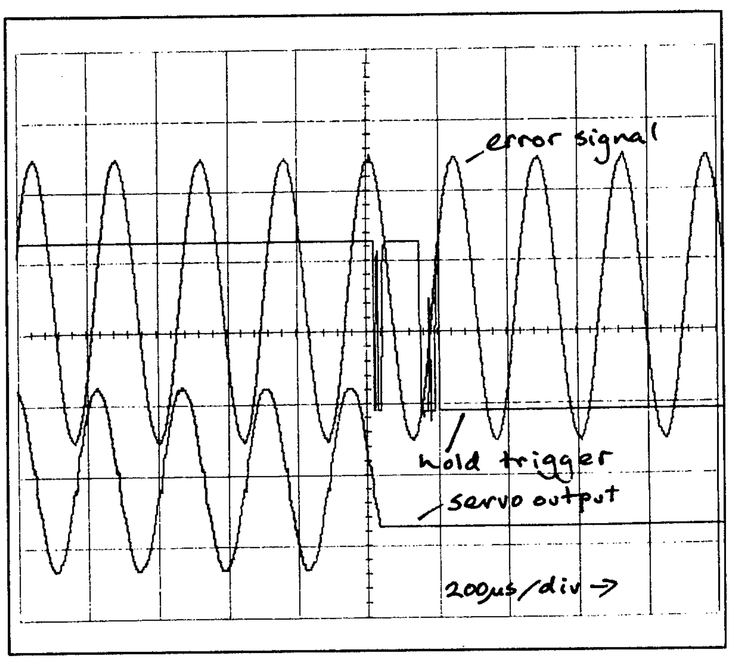

Figure 4: SERVO output: derivative control (DERIV) and 'hold' for a sinusoidal error signal

4.4.4 Type 1 and type 2 servo control and MOD

Use of INT1 as loop filter gives a type 1 servo, which tracks static 'displacement' phase perturbations with no phase error, but gives an error proportional to rate of phase change 'velocity'. Use of both INT1 and INT2 gives a type 2 response, which *can* gives zero error for both displacement and velocity type stimuli, but gives an error proportional to an 'acceleration' signal.

This was illustrated by adding a triangular wave disturbance signal to the control loop, via MOD. The results are shown in figure 9. The servo is initially type 2, and the only significant phase error is the acceleration error, consisting of spikes at the extrema of the sawtooth. Then INT2 is disabled and the type 1 velocity error produces a square-wave modulation on the output phase.

4.4.5 Sweep

The modulation signal and interferometer output for a single sweep are shown in figure 10. The servo successfully regained phase lock after sweeping.

4.4.6 Skip

Figure 11 shows the effect of a single skip: the servo shifts its lock position by 6 fringes, and regains lock afterwards. Figure 12 shows the effect of a two skips of opposite polarity in succession—the interferometer return to its original lock position.

5 Conversion of prototype to final version

The prototype will now be converted into the deliverable Fiber Phase Controller by carrying out the following work:

1. Incorporation of remaining modifications.
2. Assembly of boards into permanent enclosures.
3. Production of printed front and rear panels.
4. Construction of detectors.
5. Final testing and verification.
6. Production of final report. This will include comprehensive instructions for use of the MFPC.

6 Conclusion

A prototype Fiber Phase Controller, as described in proposal Controller for Fiber Optic Interferometer of 21st December 1992, has been constructed and tested. A description of the Fiber Phase Controller has been given and test results have been reported. This report constitutes the first deliverable item of this project.

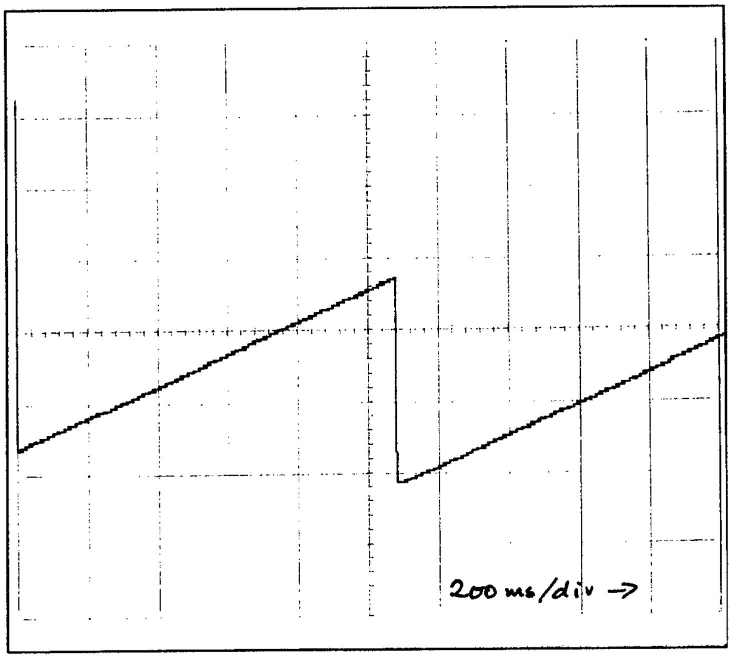

Figure 5: SERVO output: 'reset' during integrated (INT1) DC signal.

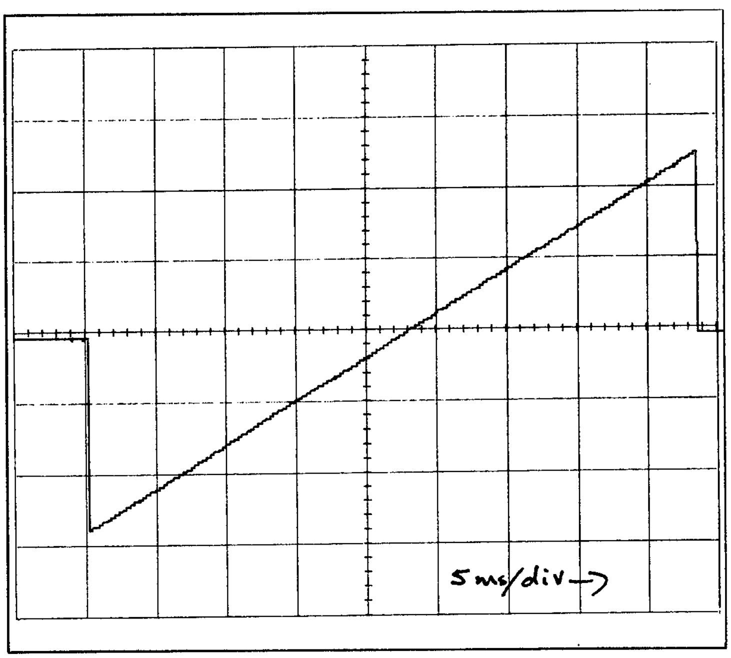

Figure 6: SERVO output: typical SWEEP

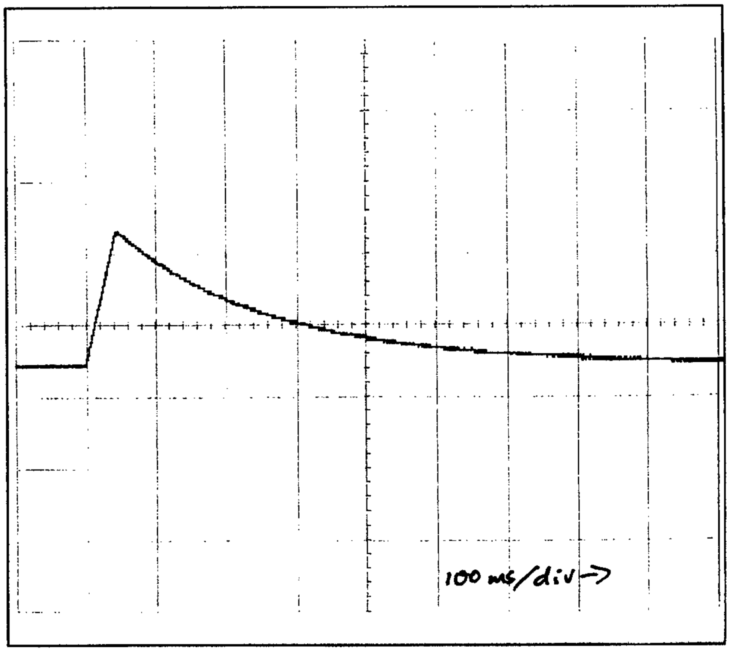

Figure 7: SERVO output: typical SKIP

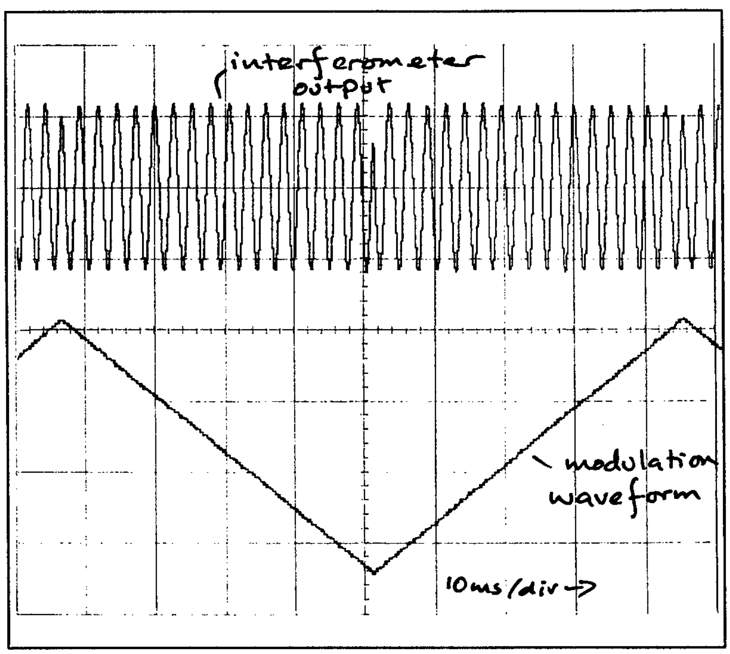

Figure 8: HVA ÷50 output and interferometer output for triangular wave phase modulation

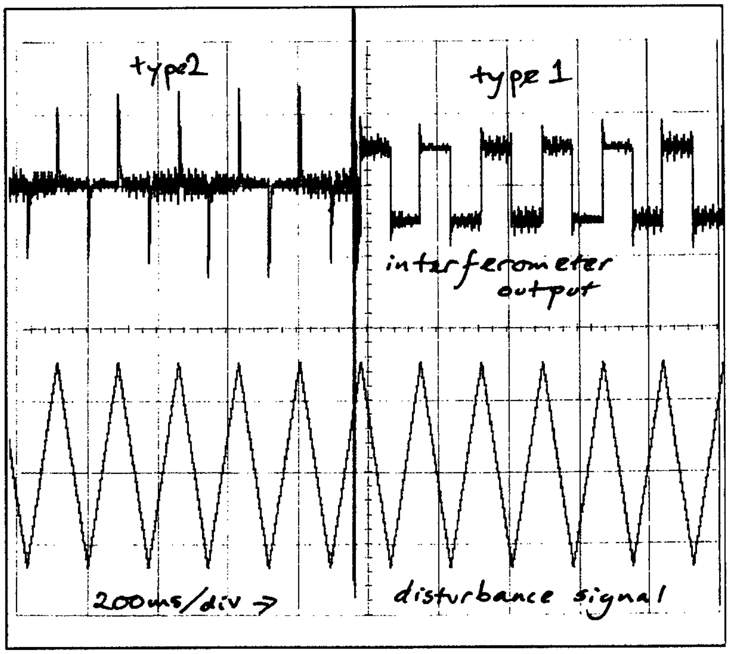

Figure 9: Type 2 and type 1 servo response for triangular phase disturbance

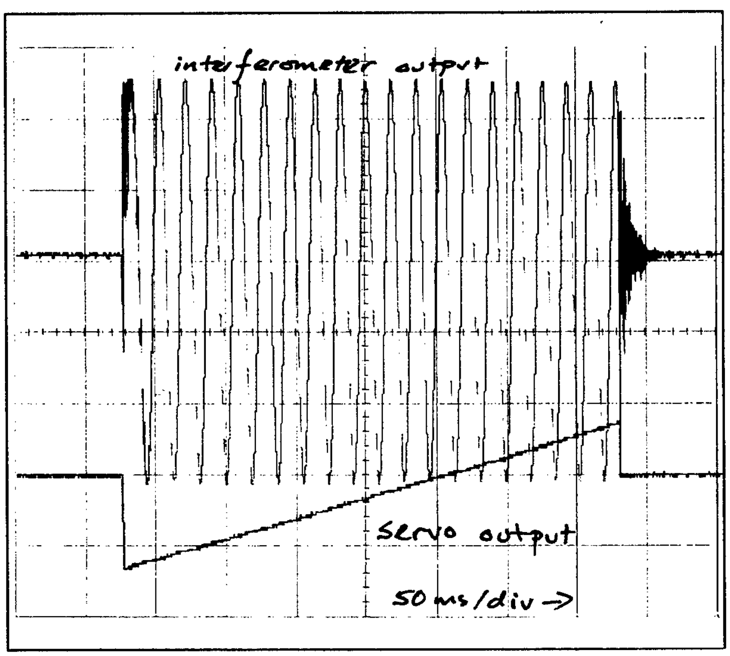

Figure 10: SWEEP applied to phaselocked system

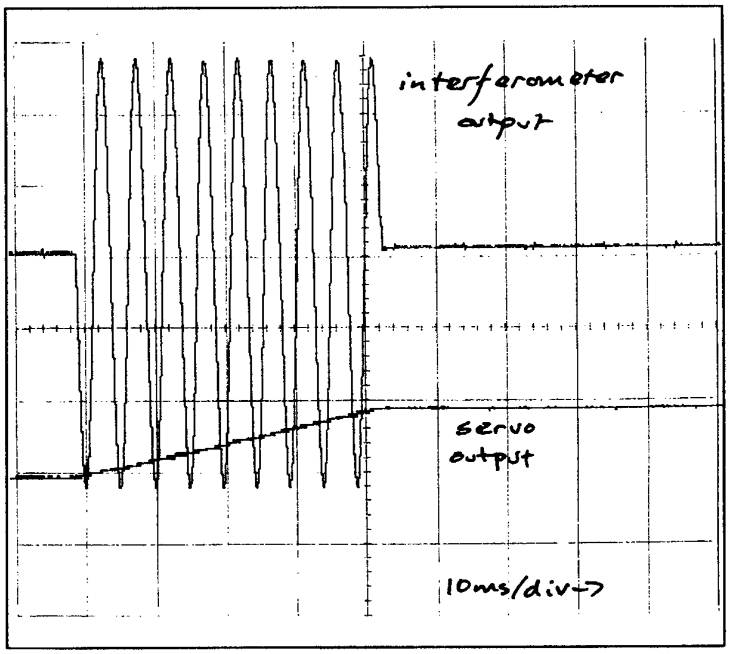

Figure 11: SKIP applied to phaselocked system

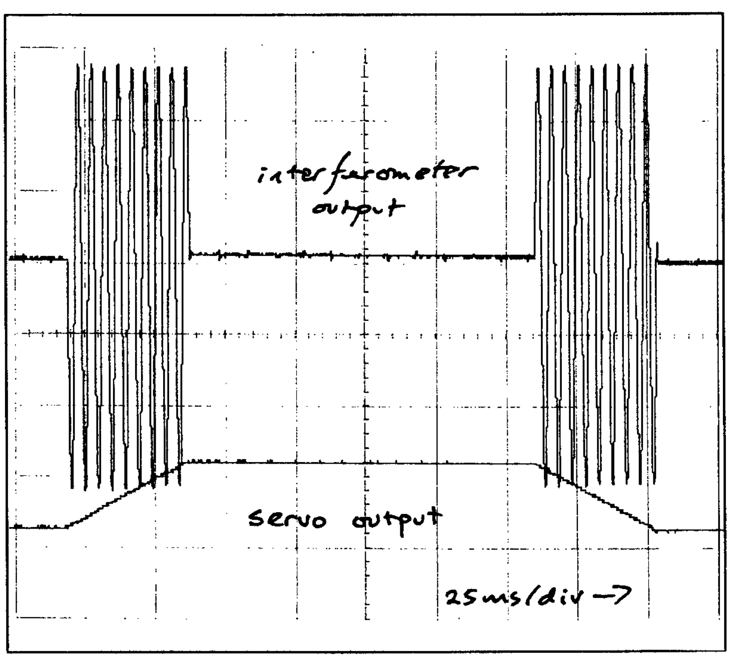

Figure 12: Two successive SKIPs of opposite polarity applied to phaselocked system